AMENDMENTS TO THE SPECIFICATION

Please replace the original title, "PSEUDO-LRU FOR A LOCKED CACHE," with the title, "CACHE-ACCESSING SYSTEM HAVING A BINARY TREE."

Please replace the paragraph beginning on page 1, line 2 of the original Application with the following paragraph:

--"This application relates to co-pending U.S. patent applications entitled "SOFTWARE-CONTROLLED CACHE SET MANAGEMENT" (Application No. 10/655,367, Docket No. AUS920020474US1) and "IMPLEMENTATION OF A PSEUDO-LRU ALGORITHM IN A PARTITIONED CACHE" (Application No. 10/655,401, Docket No. AUS920020475US1), filed concurrently herewith."—

Please replace the paragraph beginning on page 7, line 25 of the original Application with the following paragraph:

--"However, if the tag indicia of the L1 instruction cache 130 indicates that the desired information is not stored in the L1 instruction cache 130, the address register 120 sends the requested address to an L2 address register 150 to determine whether the requested information is in the L2 cache 170 instead. Furthermore, if the tag information of the L1 instruction cache 130 indicates that the desired information is not stored in the L1 instruction cache 130, the requested address is sent to the range register 140. Similarly, a miss in the L1 data cache 135 sends the corresponding address to the range register 145 and a request to the L2 address register 150. In the event of a miss of the L1 data ~~cache~~ register 125, the desired data address derived from the instruction register 120 is

transmitted to the data range register 145. Generally, the data address register 125 is then multiplexed with the output of the instruction register 120, in the L2 register 150, in the event of a miss of the L1 data cache 135."--